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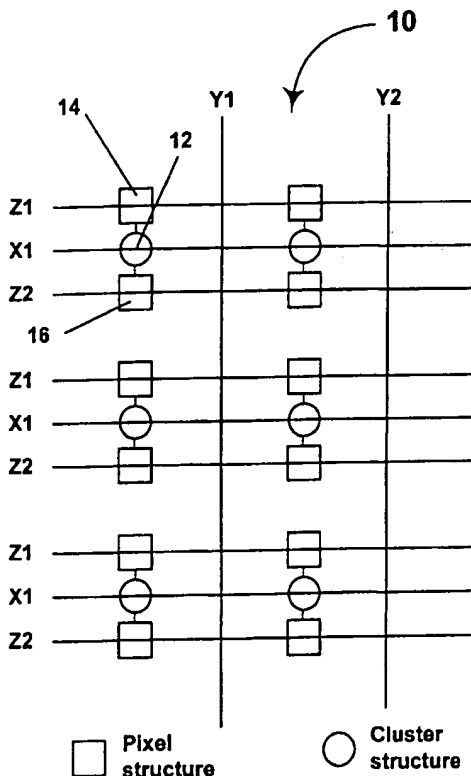
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- (71) Applicant: **E INK CORPORATION** [US/US]; 733 Concord Avenue, Cambridge, MA 02138-1002 (US).
- (72) Inventors: **COMISKEY, Barrett**; 346 Putnam Avenue, Cambridge, MA 02139 (US). **WILCOX, Russell, J.**; 17 Winnemay Street, Natick, MA 01760 (US).
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(54) Title: ADDRESSING SCHEMES FOR ELECTRONIC DISPLAYS



(57) Abstract: An electronic display comprises an electro-optic material (preferably an electrophoretic medium) having a plurality of pixels (14, 16), and separate first (X1), second (Y1, Y2) and third (Z1) sets of addressing means for addressing these pixels. Each of the pixels is associated with one addressing means in each of the three sets, such that addressing of any specific pixel requires application of signals within predetermined ranges to each of the three addressing means associated with the specific pixel being addressed.



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ADDRESSING SCHEMES FOR ELECTRONIC DISPLAYS

The present invention relates to addressing schemes for electronic displays, that is to say displays which use a display medium at least one optical characteristic of which can be varied by subjecting the medium to an electric field.

5 Electronic displays comprise a layer of electro-optic material, a term which is used herein in its conventional meaning in the art to refer to a material having first and second display states differing in at least one optical property, the material being changed from its first to its second display state by application of an electric field to the material. The optical property is typically color perceptible to
10 the human eye, but may be another optical property, such as optical transmission, reflectance, luminescence or, in the case of displays intended for machine reading, pseudo-color in the sense of a change in reflectance of electromagnetic wavelengths outside the visible range.

 One important sub-group of electronic displays are electrophoretic
15 displays, which have been the subject of intense research and development for a number of years. Such displays can have attributes of good brightness and contrast, wide viewing angles, state bistability, and low power consumption when compared with liquid crystal displays. (The terms "bistable" and "bistability" are used herein in their conventional meaning in the art to refer to displays comprising display
20 elements having first and second display states differing in at least one optical property, and such that after any given element has been driven, by means of an addressing pulse of finite duration, to assume either its first or second display state, after the addressing pulse has terminated, that state will persist without power for at least several times, for example at least four times, the minimum duration of the
25 addressing pulse required to change the state of the display element.) Nevertheless, problems with the long-term image quality of these displays have prevented their widespread usage. For example, particles that make up electrophoretic displays tend to settle, resulting in inadequate service-life for these displays.

 Numerous patents and applications assigned to or in the names of the
30 Massachusetts Institute of Technology and E Ink Corporation have recently been

published describing encapsulated electrophoretic media. Such encapsulated media comprise numerous small capsules, each of which itself comprises an internal phase containing electrophoretically-mobile particles suspended in a liquid suspension medium, and a capsule wall surrounding the internal phase. Typically, the capsules
5 are themselves held within a polymeric binder to form a coherent layer positioned between two electrodes. Encapsulated media of this type are described, for example, in U.S. Patents Nos. 5,930,026; 5,961,804; 6,017,584; 6,067,185; 6,118,426; 6,120,588; 6,120,839; 6,124,851; 6,130,773; 6,130,774; 6,172,798; 6,177,921; 6,232,950; 6,241,921; 6,249,271; 6,252,564; 6,262,706; 6,262,833; 6,300,932; and
10 6,312,304, and in International Applications Publication Nos. WO 97/04398; WO 98/03896; WO 98/19208; WO 98/41898; WO 98/41899; WO 99/10769; WO 99/10768; WO 99/10767; WO 99/53373; WO 99/56171; WO 99/59101; WO 99/47970; WO 00/03349; WO 00/03291; WO 99/67678; WO 00/05704; WO 99/53371; WO 00/20921; WO 00/20922; WO 00/20923; WO 00/26761; WO
15 00/36465; WO 00/38000; WO 00/38001; WO 00/36560; WO 00/20922; WO 00/36666; WO 00/59625; WO 00/60410; WO 00/67110; WO 00/67327 WO 01/02899; WO 01/07691; WO 01/08242; WO 01/17029; WO 01/17040; and WO 01/80287.

An encapsulated, electrophoretic display typically does not suffer
20 from the clustering and settling failure mode of traditional electrophoretic devices and provides further advantages, such as the ability to print or coat the display on a wide variety of flexible and rigid substrates. (Use of the word "printing" is intended to include all forms of printing and coating, including, but without limitation: pre-metered coatings such as patch die coating, slot or extrusion coating, slide or
25 cascade coating, curtain coating; roll coating such as knife over roll coating, forward and reverse roll coating; gravure coating; dip coating; spray coating; meniscus coating; spin coating; brush coating; air knife coating; silk screen printing processes; electrostatic printing processes; thermal printing processes; ink jet printing processes; and other similar techniques.) Thus, the resulting display can be flexible.

Further, because the display medium can be printed (using a variety of methods), the display itself can be made inexpensively.

It has been shown that some particle-based electrophoretic are capable of gray scale and that such gray scale displays are stable not only in their extreme black and white states but also in their intermediate gray states. Methods to achieve gray states include spatial, temporal and voltage addressing methods such as dithering, time-width modulation, and voltage-height modulation. Thus, this type of display is properly called "multi-stable" rather than bistable, although the latter term may be used for convenience herein.

The bistable or multi-stable behavior of electrophoretic displays (and other electro-optic displays displaying similar behavior) is in marked contrast to that of conventional liquid crystal ("LC") displays. Twisted nematic liquid crystals act are not bi- or multi-stable but act as essentially instantaneous voltage transducers, so that applying a given electric field to a pixel of such a display produces a specific gray level at the pixel, regardless of the gray level previously present at the pixel. Furthermore, LC displays are only driven in one direction (from non-transmissive or "dark" to transmissive or "light"), the reverse transition from a lighter state to a darker one being effected by reducing or eliminating the electric field. Finally, a pixel of an LC display is not sensitive to the polarity of the electric field, only to its magnitude, and indeed to avoid undesirable effects, such as damage to electrodes, caused by current imbalance through a display, commercial LC displays usually reverse the polarity of the driving field at frequent intervals. In contrast, electrophoretic displays act as impulse transducers, so that the final state of a pixel depends not only upon the electric field applied and the time for which this field is applied, but also upon the state of the pixel prior to the application of the electric field.

The bistable or multi-stable (also sometimes referred to as "latching" or "memory") characteristics of electrophoretic displays affect the choice of addressing methods to be used with such displays. Other factors which influence the choice of addressing methods to be used include the need for DC addressing because

of the sensitivity of electrophoretic displays to the polarity of the electric field, and the desirability of DC-balanced waveforms; to avoid potentially harmful changes at the electrodes, it is desirable that the algebraic sum of the impulses applied to any given pixel of an electrophoretic display over time be zero. Also, the addressing method should allow for the lack of a threshold in electrophoretic displays; since such displays are impulse transducers, with a nearly linear relationship between (a) the product of voltage and time and (b) the change in optical characteristic of the display, even a small voltage applied for a substantial time will cause a change in the optical characteristic of the display. This normally precludes the use of passive matrix addressing methods.

Frequently, high resolution electrophoretic displays consist of pixels laid out in an array, with a transistor construction behind each pixel in a so-called "active matrix" arrangement. This arrangement can further be subdivided into sub-pixels. However all the transistors are in a plane, and control an array of bottom electrodes that are either on the same plane or on an adjacent plane just above or below. As such, the array is addressed in a two-dimensional or XY manner where pixels are referenced by row and column.

One problem with such high resolution displays is the sheer number of drivers required. In an array addressed in an XY manner, if there are x columns and y rows, x + y drivers are needed to address x*y pixels. For example, a color 640 x 480 display with three sub-pixels per pixel has $640 \times 480 \times 3 = 921,600$ pixels and would typically be addressed by 480 row drivers and 1920 column drivers for a total of 2400 display drivers. Especially in small displays, the cost of the drivers rivals or may outweigh the cost of the electro-optic material.

In one aspect, the present invention provides an electronic display which reduces the number of drivers required.

Another problem with such high resolution displays is the time taken to address the display. Normally, in an active matrix display, one row of the display is activated at a time, and all the pixels in that row are addressed by applying appropriate voltages to the various columns. If addressing one row takes k seconds,

at least $k \cdot y$ seconds are required to address the complete display. If the addressing scheme used requires that each row be addressed for the time necessary to completely address an electrophoretic medium (which is typically of the order of 100 milliseconds), the total time taken to address the display may be undesirably great. Similar considerations apply to displays using other types of electro-optic materials.

In another aspect the present invention provides various methods for reducing the time needed to completely address an electronic display.

Accordingly, in one aspect, this invention provides an electronic display comprising an electro-optic material having a plurality of pixels, and separate first, second and third sets of addressing means for addressing the pixels, each of the pixels being associated with one addressing means in each of the three sets, such that any specific pixel of the display can be addressed by application of signals within predetermined ranges to each of the three addressing means associated with that specific pixel.

This invention also provides an electronic display comprising an electro-optic material having a plurality of separately addressable pixels, wherein the number of driver outputs to the pixels is less than the square root of the number of pixels.

In another aspect, this invention provides a method of addressing an electronic display, the method comprising:

- providing an electro-optic material having a plurality of pixels;
- providing first, second and third sets of addressing means for addressing the pixels, each of the pixels being associated with one addressing means in each of the three sets; and

- applying predetermined signals to the three addressing means associated with a specific pixel, thereby addressing this pixel.

This type of addressing method will hereinafter be called "three-dimensional addressing" and the corresponding display may be called a "three-dimensional display", it being understood that this does not necessarily imply that

the pixels of the display have substantial extent in all three dimensions; for example, the pixels might be arranged in a large planar array, but electrically grouped into sub-arrays for purposes of addressing the display, with the selection of any one sub-array being made by the third set of addressing means.

5 In another aspect, this invention provides a method of addressing a bistable electronic display having a plurality of pixels arranged in an array comprising a plurality of rows and plurality of columns, the method comprising selecting a plurality of rows or columns and applying a simultaneous and equivalent switching impulse to all selected rows and columns.

10 In another aspect, this invention provides a method of addressing a bistable electronic display having a plurality of pixels arranged in a plurality of rows, the method comprising:

15 (a) comparing a starting state of the display with a desired finishing state and determining for each pixel a change value representative of the change needed to change the starting state of that pixel to its desired finishing state; and

20 (b) calculating from the pixel change values for each row, a switch direction value for that row, this switch direction value representing the value for which, if all pixels of that row were changed by the switch direction value, the row switch time required to switch the row to the desired finishing state would be minimized.

 This method may also include any one or more of the following steps:

 (c) calculating the average switch direction value for all rows of the display;

25 (d) identifying all rows with switch direction values less than the average switch direction value calculated in step (c);

 (e) calculating the average switch direction value of all rows identified in step (d);

(f) applying to all rows identified in step (d) an impulse sufficient to cause a change in state equal to the average switch direction value calculated in step (e);

5 (g) identifying all rows with switch direction values greater than the average switch direction value calculated in step (c);

(h) calculating the average switch direction value of all rows identified in step (g); and

10 (i) applying, to all rows identified in step (g), an impulse sufficient to cause a change in state equal to the average switch direction value calculated in step (g).

15 In another aspect, this invention provides a method of addressing a bistable electronic display having a plurality of pixels, each of these pixels having a first display state, a second display state differing in at least one optical characteristic from the first display state, and a plurality of intermediate states having values of this optical characteristic intermediate those of the first and second display states. The method comprises driving all the pixels of the display to the same one of the intermediate states; and thereafter addressing the pixels individually to drive them to their desired states.

20 In another aspect, this invention provides a method of addressing a bistable electronic display having a plurality of pixels arranged in a plurality of rows and columns. The method comprises:

(a) comparing a starting state of the display with a desired finishing state and determining for each pixel a change value representative of the change needed to change the starting state of that pixel to its desired finishing state;

25 (b) comparing the change values of pixels in differing rows but the same column and locating at least two of these pixels having the same change value; and

30 (c) addressing these at least two pixels having the same value simultaneously by addressing the rows and the column on which these pixels are located.

In another aspect this invention provides a method of addressing a bistable electronic display having a plurality of pixels, the method comprising comparing a starting state of the display with a desired finishing state and determining which pixels differ between the two states; and addressing only those
5 pixels which differ between the two states.

Finally, this invention provides a of addressing a bistable electronic display having a plurality of pixels. This method comprises:

providing an array of island capacitors associated with the pixels of the display;
10 through passive matrix XY addressing, introducing electrical charge into the capacitors in a pattern matching the image desired on the display; and thereafter allowing the charges on the capacitors to complete the addressing of the pixels of the display.

Figures 1, 2 and 3 of the accompanying drawings are schematic circuit diagrams of first, second and third three-dimensionally addressed displays of
15 the present invention;

Figure 4 is a schematic circuit diagram of a fourth three-dimensionally addressed display of the present invention having the form of a multi-page electronic book;

20 Figures 5A and 5B illustrate one method of providing addressing means in the type of display shown in Figure 4 and in a similar display; and

Figures 6-10 illustrate five different three-dimensionally addressed displays of the present invention, all of which use a photoconductor as part of an addressing method using light sources and light valves.

25 The accompanying drawings are highly schematic and not to scale, emphasis instead generally being placed upon illustrating the principles of the invention.

As already mentioned, the three dimensional displays and methods of the present invention use an electro-optic material having a plurality of pixels, and
30 separate first, second and third sets of addressing means for addressing the pixels.

In this display and method, each of the pixels is associated with one addressing means in each of the three sets, such that addressing of any specific pixel requires application of signals within predetermined ranges to each of the three addressing means associated with that specific pixel. The additional dimension is accomplished
5 by introducing a method of addressing sub-arrays within the array. By thus substituting a three-dimensional addressing scheme for a two-dimensional one, the number of drivers can be greatly reduced. In effect, the present invention splits the display into z regions, each addressable by the x columns and y rows, enabling the entire display of $x*y*z$ pixels to be addressed by $x + y + z$ drivers. For example, the
10 aforementioned color 640 x 480 display with three sub-pixels per pixel could be addressed by 64 columns and 240 rows replicated across 60 regions for a total of 364 drivers for the same 921,600 pixels, reducing driver cost substantially. In this and many other cases of practical interest, the present invention enables the number of drivers (or more accurately driver outputs), to be reduced to less than the square
15 roots of the number of pixels in the display, a highly desirable result which cannot be achieved by conventional addressing methods. The additional dimension may comprise only a logical sub-array, or may include a physical sub-array that may even comprise an additional layer in the display stack.

In the three-dimensional display of the present invention, in which
20 the pixels are arranged in a plurality of sub-arrays, each pixel within any specific sub-array can be associated with one of the first and second sets of addressing means, and the third set of addressing means can have the form of a plurality of switching means, at least one of which is associated with each sub-array, the switching means associated with each sub-array having an off state, in which signals
25 on at least one of the first and second sets of addressing means are prevented from reaching the associated sub-array, and an on state, in which signals from both the first and second sets of addressing means are permitted to reach and address the associated sub-array. Such a display may have control means arranged to control the switching means so that only the switching means associated with one sub-array is
30 in its on state at any given moment.

Thus, for example, the additional layer of logic may consist of a platform hierarchy. In this hierarchy, one transistor may act as a gate that controls additional transistors. This may be accomplished physically by wiring a cluster of transistors to a central transistor. The central transistor may be in the same plane as the pixel transistors or may be in a different layer but still in electrical communication. In this approach the cluster-level transistor and the pixel-level transistor can be individual transistors or whole logic structures capable of some degree of intelligence and processing. The cluster transistors may be addressed in an XY manner with an addressing signal that communicates how the sub-array should be addressed. This hierarchy may be repeated in multiple logical or physical layers, permitting many pixels to be addressed by a few central transistors.

Because of the bistable nature of electrophoretic displays, one way to utilize the hierarchy involves first setting the cluster logic structures to open electrical communication to one (or a subset in parallel) of the downstream pixels. These pixels are then addressed by an XY scan. The clusters are then reset to open communication with a different set of downstream pixels. These pixels are then addressed by an XY scan; however the image from the first set of pixels is not lost because it remains visible even when not being addressed.

In one form of the invention using sub-arrays, each sub-array comprises a discrete page, the pages formed by the plurality of sub-arrays being stacked on top of each other so that the entire display forms a multi-page electronic book. Thus, this invention provides economical devices that look and feel like multi-page books. Such a book may have conductive vias extending between adjacent pages and connecting at least one of the first and second sets of addressing means on the adjacent pages. A display of this type is described below with reference to Figure 4. Alternatively, each sub-array may correspond to a different column in a newspaper, and thus the present invention provides a large paper-like display the size of a newspaper broadsheet that may be economically addressed.

As already indicated, in the three-dimensional display of the present invention, the first second and third sets of addressing devices can all have the form

of electrical conductors and/or electronic devices, typically transistors. However, the present invention is not restricted to this purely electrically or electronic approach. In another approach, the operation of sub-arrays within a basic pixel array are made contingent on an external gate based on temperature, light, vibration, magnetism, radio waves, or other suitable force. For example, suppose the pixel-level logic structures comprise microelectromechanical system (MEMS) devices with a see-saw switch that cannot move in the presence of a magnetic field. An array of such structures is addressed with XY coordinates. However, adjacent to such array is a layer of material capable of emitting a magnetic field, this layer being divided into halves. When only one half is active, only half the display can be addressed. Suppose that the Y addressing means are wired in parallel so that activating the Yth column activates two columns, one in each half. Only the column not in the magnetic field actually causes switching to occur. In this manner, the magnetic layer provides another addressing dimension, permitting three-dimensional addressing.

The three-dimensional addressing methods of the present invention may be especially useful when at least one of the sets of addressing devices makes use of a photoconductor. The display may comprise a light source (for example, a light-emitting layer) associated with the photoconductor and selectively operable to switch the photoconductor between a conductive and a non-conductive state. The light source may be an electroluminescent material. Alternatively, the display may comprise a light source associated with the photoconductor and a light valve disposed between the light source and the photoconductor and arranged to control transmission of light from the light source to the photoconductor. Any suitable light valve maybe used, including light valves operating by use of polymer-dispersed liquid crystal (PDLC), suspended particle and electrochromicity. A PDLC light valve is a preferred embodiment due to the relative ease of obtaining thin sheets of such media at low cost.

Although using light valves has the disadvantages that a large proportion of the light emitted from the light-emitting layer is wasted, reducing

device lifetime, and an additional layer is required, thickening the medium and complicating manufacture, these disadvantages tend to be outweighed by the major advantage that light valve layers can be made inexpensive and flexible.

There are a variety of arrangements available with light valves. For example, in one embodiment, the display may comprise a plurality of light sources arranged as a series of elongate rows, and a plurality of light valves arranged as series of elongate columns crossing the elongate rows, the light sources and light valves together defining a two-dimensional array of pixels in the photoconductor. In another embodiment, the display may have the form of a plurality of pages stacked on top of one another to form a multi-page electronic display, and each page may have a single light source and a single light valve, so that the page or pages to be written at any given moment are selected by controlling the state of the light valves. In a further embodiment, the first addressing means comprises a plurality of electrical conductors and means for applying potentials selectively to these conductors, the second addressing means comprises a plurality of light emitting devices and means for generating light selectively from these light emitting devices, and the third addressing means comprises a plurality of light valves and means for selectively setting these light valves to their transmissive or non-transmissive states.

One convenient application of the three-dimensional addressing schemes of the present invention is in electronic displays having three sets of pixels arranged to display different colors. In this type of display, the third set of addressing means may be arranged to select one of the three sets of pixels to be addressed at any given moment. A display of this type is described below with reference to Figure 8.

The present display and method are not restricted to the use of only three dimensions for addressing. A display of the present invention may comprise a fourth set of addressing means for addressing the pixels, this fourth set being separate from the first, second and third sets of addressing means. Each of the pixels of the display is associated with one addressing means in each of the four sets, such that any specific pixel of the display can be addressed by application of signals

within predetermined ranges to each of the four addressing means associated with that specific pixel, thus providing a four-dimensional addressing scheme. For example, in the embodiment of the invention described above which simulates a broadsheet newspaper, it may be convenient to divide the large display into a two-dimensional grid of sub-arrays, each sub-array being addressed in the conventional XY manner by the first and second sets of addressing means, while the selection of the sub-array to be addressed at any given moment is controlled, also in an XY manner, by the third and fourth sets of addressing means.

As already indicated, the electro-optic material used in the display of the present invention is preferably an electrophoretic medium, most desirably an encapsulated electrophoretic medium, as described in the aforementioned patents and published applications. The present invention requires no modification of the electrophoretic medium itself, so the preferred media will not be described in detail herein, the reader being referred to the aforementioned patents and published applications which describe the preferred electrophoretic media in detail. Other types of electro-optic materials could also be used. The electro-optic medium could, for example, be of the rotating bichromal object type as described, for example, in U.S. Patents Nos. 5,803,783; 5,777,782 and 5,760,761. The medium could also be any of the class of electrochromic and suspended particle displays. Other types of electro-optic materials, include, for example, liquid crystal, especially polymer-dispersed and/or reflective liquid crystal, and suspended rod-shaped particle devices; see Saxe, Information Display, April/May 1996 (Society for Information Display), and US Patent No. 4,407,565.

Embodiments of the invention will now be described, though by way of illustration only, with reference to the accompanying drawings.

As already indicated, XYZ addressing can be accomplished when there is a separate method of addressing or affecting the cluster-level transistor structures, aside from the conventional XY array. One very simple example of such addressing is shown in Figure 1 of the accompanying drawings. This Figure shows a first display of the present invention (generally designated 10) having row drivers

X1, X2, X3 and column drivers Y1, Y2. Cluster structures 12 are provided connected to the row drivers X1, X2, X3, these cluster structures each having a first and second states. When the cluster structures 12 are in their first state, they connect the row drivers X1, X2, X3 to the odd lines of the display, designated Z1, thus enabling addressing of pixels 14 located on these odd rows, and isolate the row drivers from the even lines of the display, designated Z2. On the other hand, when the cluster structures 12 are in their second state, they connect the row drivers X1, X2, X3 to the even lines Z2 of the display, thus enabling addressing of pixels 16 located on these even rows, and isolate the row drivers from the odd lines Z1 of the display 10. This logic occurs at the cluster structure (or in such a simple example, could also occur by simply by wiring X and Z together at the pixel structure and splitting the necessary threshold activation voltage in half between them). Thus, the display 10 achieves XYZ addressing that functions in a manner similar to interlacing.

Figure 2 illustrates a second display (generally designated 20) using a variation of the same approach. In this display 20, a single line Z connected to the clusters 12 can vary between two values, say 0 and 1. The cluster logic is such that when the Z value is 0, the input on row drivers X1, X2, X3 affects the pixels above (in Figure 2) the clusters 12, but when the Z value is 1, the input on row drivers X1, X2, X3 affects the pixels below the clusters 12.

As already noted, the three-dimensional addressing method of the present invention is particularly useful with displays using photoconductors for addressing. It has previously been proposed to address electronic display media by means of light impinging upon a photoconductor; see, for example, Blazo, High Resolution Electrophoretic Display with Photoconductor Addressing, SID Digest, 1982, pages 92-93, and the aforementioned International Application Publication No. WO 99/47970 of E Ink Corporation. In one such addressing scheme (hereinafter for convenience called the "row light-emitter scheme"), the display comprises in sequence:

- (a) a first transparent electrode, typically formed from indium tin oxide (ITO), which is patterned into columns;
- (b) the display medium itself, which may be an electrophoretic display medium, preferably an encapsulated electrophoretic display medium;
- 5 (c) a photoconductor layer;
- (d) a second, light-transmissive electrode in electrical contact with the photoconductor layer; and
- (e) a light-emitting layer patterned into rows.

Whenever a row of the light-emitting layer is activated, the corresponding region of
10 the photoconductor is able to conduct current and the columns of the first electrode can control the image of that row. This embodiment is appropriate when the light source (e.g. an electroluminescent (EL) light source) does not have a threshold. One drawback of this approach is that the light from each row must stay on for all or most of the time required for the display medium to image. If this takes k seconds, it
15 may require up to $k \cdot y$ seconds to address y rows.

In a second such addressing scheme (hereinafter for convenience called the "pixelated light-emitter scheme"), the first electrode is not patterned, and the light-emitting layer is pixelated (i.e., patterned into a two-dimensional grid of individually controllable pixels) so that it can apply any desired image to the
20 photoconductor layer. Where light is present, the photoconductor layer conducts current, the corresponding portions of the display medium experience an electric field and the display medium is imaged accordingly. Provided the display medium used is bistable, the light-emitting layer may then be switched off until the image needs to be changed. This addressing scheme is especially useful when the light
25 source (e.g. organic light-emitting diodes (OLED's)) has a threshold and may be passively addressed. An advantage of this approach is that the light pattern is applied across all rows simultaneously and only k seconds are required to address y rows. A disadvantage is that only certain light-emitting materials may be easily multiplexed.

As already noted, both addressing schemes require numerous drivers, for example 2400 drivers for a full color 640 x 480 display, and in small displays especially the cost of the drivers rivals or may outweigh the cost of the electro-optic material. The present invention enables the number of such drivers to be greatly
5 reduced by forming separately addressable regions or sub-arrays. Such separately addressable regions may be formed in several ways.

Figure 3 illustrates one way of forming such separately addressable regions. This Figure shows a third display of the present invention (generally designated 100) having a first region comprising rows 102, 104 and 106 and a
10 second region comprising rows 112, 114 and 116. Each row is connected to a driver 118, the rows 102 and 112 being connected via a driver line 122, the rows 104 and 114 by a driver line 124, and the rows 106 and 116 by a driver line 126. Each row is provided with a logic element 128 or 130, such as a transistor, that governs whether voltage reaches the light-emitting region of a row. As shown in Figure 3, several
15 rows in different regions may be wired to a common driver line, yet only a combination of voltage across a row and voltage to the associated transistor will result in light emission from any given row.

Also, as already indicated, the separately addressable regions may be separate sheets of the display medium, as illustrated in Figure 4. This Figure shows
20 a fourth display (generally designated 50) of the invention having the form of a multi-page electronic book; although only two pages P1 and P2 are shown in Figure 4, more pages would normally be present. Each page is provided with a set of row electrodes r1, r2, r3 under the control of row drivers (not shown). The row electrodes r1, r2, r3 on the various pages are connected the rows in parallel, each
25 row electrode passing through a conductive pad 52, which extends through the pages of the display medium as a via. When the individual pages are placed adjacent and in approximate registration with each other (much like a bound book) the vias extend from the top page to the bottom page in electrical connection. Any suitable means of providing this connection may be employed, such as anisotropic tapes,
30 zebra strips, conductive glues, and the like. Any suitable means of via formation

(whether at the step where each sheet is constructed or afterwards to create a via through all sheets) may be employed. The pages P1, P2 are provided with column electrodes under the control of column drivers, both the column electrodes and the column drivers being omitted from Figure 4 for ease of illustration. The column electrodes on the various pages are also connected in parallel by vias in the same way as the row electrodes. The third set of addressing means in the display 50 comprises a set of transistors 54, one of which is provided in each row electrode r1, r2, r3 in each page of the display. The transistors 54 are controlled by control lines z1, z2, all of the transistors on any one page being on or off simultaneously.

The display 50 operates in the following manner. One row electrode (say r1) is selected in the usual manner, and because of the presence of the vias 52 this selects r1 on each page P1, P2. However, the transistors 54 on only one of the pages P1, P2 are turned on, so that the portion of the row electrode r1 adjacent the electrophoretic medium (not shown) is selected on only one page. Accordingly, when appropriate voltages are placed on the column electrodes, only the selected row on the selected page is addressed.

Figure 5A illustrates a convenient method of forming the transistors 54 used in Figure 4, or any other display using similar transistor arrays. One benefit of the display 50 shown in Figure 4 is that the transistors are all present in narrow strips on each page. Accordingly, as shown in Figure 5, the necessary transistors may be formed by any conventional process on a sheet 60, which is then cut, as indicated by the broken lines 62, to form multiple transistor strips 64. The individual pages of the display 50 are prepared in the form shown in Figure 5A with the individual row electrodes broken where the transistors 54 are to be inserted, and the adjacent ends terminated in conductive pads 66. The transistor strip 64 is then secured in position on the page to form the completed structure shown in Figure 4.

The strip 64 need not be formed on a flexible substrate. For example, a thin, inflexible strip placed in a column orientation as shown in Figure 5A would not interfere with the flexibility of the visible portion of the display medium, since the strip 64 can be placed in a region corresponding to the spine and binding of a

conventional book. The transistors in the strip 64 could also be combined with on-board drive logic, such as shift registers. In this way, each transistor could be separately addressed, either eliminating the need for row drivers or reducing the number of drive lines required.

5 The transistors 54 shown in Figure 4 need not be formed by the process of Figure 5A; the transistors may be placed onto the sheets of medium by any suitable means. For flexible media, thin film transistors (TFT's) on a flexible substrate (whether amorphous silicon or polycrystalline silicon) and including methods like flexible integrated circuits, organic TFT's, and the method of
10 International Application Publication No. WO 96/41372 are all suitable. Alternatively, transistor formation could be performed directly on the sheet substrate.

Figure 5B shows a variation of the method of Figure 5A which may be useful in forming the photoconductor-containing displays discussed below. As
15 shown in Figure 5B, on a page P, which will eventually form part of a multi-page display, a single row electrode r1 is connected to a plurality of electroluminescent strips 70; only three strips 70 are shown, but more would of course normally be used. The connections between row electrode r1 and strips 70 are broken where
20 transistors are to be inserted, the ends adjacent the break being terminated by conductive pads 72. To produce the finished page P, a transistor strip 74, formed in the same manner as in Figure 5A, is secured across the breaks in the connections. Note that unlike the transistor strip 62 shown in Figure 5A, in which all the transistors switch off or on simultaneously, the strip 74 requires that its transistors be individually controllable, so that a single strip 70 can be selected for operation.

25 As already indicated, one approach to three-dimensional addressing substitutes light valves for transistors or similar logic elements in at least one of the "dimensions" of the addressing. The light valve may be used in association with elongate light sources. Light may be emitted from all the elongate light sources which are wired in parallel, but the light valve layer is introduced between the light
30 sources and the photoconductor layer, so that this light valve layer governs whether

the light reaches the photoconductor. The embodiments of the invention shown in Figures 6-10 are all of this type.

Figure 6 shows one page (generally designated 200) of a display of the present invention, this page comprising, in order, an electroluminescent (EL) layer 202, a polymer-dispersed liquid crystal (PDLC) light valve layer 204, a photoconductor layer 206, an electrophoretic medium layer 208 and an indium-tin oxide (ITO) layer 210; the layer 210 is normally provided on a substrate (not shown). As indicated schematically in Figure 6, the electroluminescent layer 202 is patterned into a plurality of elongate rows r1, r2, r3, r4 and the light valve layer 204 is patterned into a plurality of columns c1, c2, c3, c4 extending perpendicular to the rows. The columns c1, c2, c3, c4 are addressed directly and there is no need to pattern the top ITO layer into columns, although of course in a multi-page display the third dimension of addressing would be provided by transistor or similar devices to ensure that the ITO layer on only one page was selected at any given moment. A two-dimensional passive display is formed by the EL and PDLC columns, that emits light. The light may be emitted row-by-row, requiring $k \cdot y$ (where k and y are as previously defined) seconds to update y rows. Alternatively, if the PDLC and EL materials respond quickly relative to the photoconductor, the PDLC/EL display may be multiplexed and a complete graphical image produced that affects the photoconductor across the entire display, requiring only k seconds to update y rows.

Figure 7 shows a display (generally designated 230) which is generally similar to the display 200 shown in Figure 6, in that the electroluminescent layer is again patterned into a plurality of elongate rows r1, r2. However in the display 230, the ITO layer is patterned to form alternating columns c1, c2 (the patterned columns correspond to groups of standard column-patterned electrode-over-ink columns), while the PDLC layer is patterned into columns which occupy the width of an adjacent pair of the columns in the ITO layer. This allows high resolution which permitting the groups of alternate ITO columns to be driven in parallel, as indicated in Figure 7.

Figure 8 shows a full color display (generally designated 240) in which the electroluminescent layer is again patterned into a plurality of elongate rows r1, r2. The ITO layer is again patterned to form columns c1, c2, c3, c4, but in this case each of these columns is individually selectable. The PDLC layer is
5 patterned to form sub-columns one-third the width of the columns c1, c2, c3, c4 (although some other sub-multiple could be used), the sub-columns being arranged, as shown in Figure 8, in three cyclically-repeating groups, the sub-columns of each group being driven in parallel. The three groups of sub-columns are associated with red, green and blue sub-pixels, and thus permit interlaced updating of the three
10 colors of the display, as well as three-dimensional addressing.

Figure 9 shows a display (generally designated 250) in which the ITO layer is patterned to form individually-selectable columns c1, c2, c3, c4 in the same manner as in Figure 8. However, in the display 250, the PDLC layer is patterned to form individually-selectable rows z1, z2, orthogonal to the ITO columns c1, c2, c3, c4, while the EL layer is patterned to form sub-rows parallel to, but one-half the
15 width of, the PDLC rows. Alternate EL sub-rows are driven in parallel to achieve three-dimensional addressing.

Finally, Figure 10 shows a display (generally designated 260) which is essentially the converse of that shown in Figure 9. The ITO layer is patterned to form individually-selectable columns c1, c2, c3, c4 in the same manner as in Figures
20 8 and 9. Again both the PDLC layer and the EL layer are patterned to form rows orthogonal to the ITO columns c1, c2, c3, c4, but in this case the EL layer is patterned to form individually-selectable rows r1, r2, while the PDLC layer is patterned to form sub-rows z1, z2 parallel to, but one-half the width of, the EL rows. Alternate PDLC sub-rows are driven in parallel to achieve three-dimensional
25 addressing. This embodiment allows the achievement of row resolutions which are higher than may readily be achieved by patterning the EL layer.

It will readily be seen by those skilled in display technology that the principles illustrated by the preferred embodiments described above may be
30 employed to create many combinations and variations in addressing schemes. In

displays using electroluminescent or similar light-emitting layers, it is preferred that the time for which the light-emitting layer must be active be minimized to extend the life of the light-emitting layers. In addition, consideration must be given to the ease of patterning the respective layers into rows, columns and regions, and to the flexibility characteristics of the respective layers.

For example, one embodiment consists of column-patterned electrode-over-ink columns (in an ITO or similar layer) connected in parallel across z regions, a PDLC layer patterned in rows connected in parallel across z regions, and a light-emitting EL layer patterned into z regions, such as single pixels the size of pages of a multi-page display.

In such a display, to image, for example, row 24 on page 17, the column drivers are set at the appropriate voltage potential for black or white at this pixels in this row (the relevant potentials are applied on all pages but do not create an image change except where the photoconductor has been activated by light), all rows except row 24 are set at the voltage potential causing the PDLC to turn opaque, row 24 is set to the voltage potential allowing the PDLC to be transmissive, and the page 17 EL layer is activated. Thus, to address the entire book this way, a given page of EL material is active for only $k*y$ seconds.

For reasons which will be apparent to those skilled in typography, for applications such as imaging text in the Roman alphabet in a multi-page electronic book, it is desirable that the resolution be such that the number of columns (x) is greater than the number of rows (y); furthermore, the number of rows will typically be much greater than the number of pages (z). Hence, in a preferred embodiment, the PDLC layer is patterned into z regions, such as individual pages, while the EL layer is patterned into y rows. This corresponds to a variation of the embodiment of Figure 7 in which z_1 and z_2 are separate pages. One advantage of this embodiment is that to address the entire book, a given row of EL material is active for only k seconds while each page is addressed for $k*z$ seconds, which is less than $k*y$ seconds. Furthermore, this embodiment requires that the highest resolution be used to pattern the ITO layer, which can readily be patterned at very high resolution.

Also, pages are typically flexed from side to side but not top to bottom. In this embodiment, the relatively brittle ITO lines oriented in columns receive less physical stress than the relatively flexible EL lines oriented in rows. Indeed, stiff physical columns in or attached in connection with the display substrate could be used to heighten this protection without undue reduction in the utility of the display.

In further embodiments of the invention, the photoconductive layer could itself be patterned. In addition, the embodiments described above can readily be adapted to provide a four-dimensional (WXYZ) addressing scheme if all four addressing layers (the EL, PDLC, photoconductor and ITO layers) are patterned or if the display is split into separate physical pages, as in the display shown in Figure 4. For example, the embodiment of Figure 7, shown as covering a single page, could be replicated across multiple pages, with an additional set of addressing means provided to select the page to be written at any given moment.

Until now, it has been assumed that the light-emitting layers used in the preferred embodiments described above do not have a threshold for light emission. Consideration will now be given to the somewhat simpler case in which the light-emitting layer has a threshold, such that light emits only above a voltage potential V .

It will readily be seen that the addressing methods suitable for a non-threshold light-emitting layer (and combinations and variations thereof) may also be used with a threshold light-emitting layer. The threshold characteristic however provides an additional degree of freedom and enables three-dimensional addressing to be accomplished with fewer physical layers (or conversely permits a four or more-dimensional addressing scheme if enough patterned layers are present).

Given a threshold light-emitting layer, an addressable sub-array (z region) may be formed as follows. The bottom electrode of the light-emitting layer is patterned for example in rows. The top clear electrode of the light-emitting layer is patterned into z regions (as above, these regions may be correspond to groups of columns, groups of rows, sub-columns, sub-rows or discrete pages, or variations and combinations thereof). As a voltage of $V/2$ is applied to a row in parallel across

each of the z regions, a voltage of $-V/2$ is applied to any z region that needs to be addressed. This establishes the V potential difference and light is emitted only for the row(s) in that region.

For example, suppose a line r1 addresses the 10th row bottom
5 electrode of the light-emitting layer on all pages of an electronic multi-page book. A common top electrode of the light-emitting layer on the 14th page is activated with $-V/2$. Only the 10th row of the 14th page is imaged.

In a further embodiment, the light-emitting layer is patterned into columns and rows, for example in the form of a passive-OLED display. Multiple
10 pages are provided with rows and columns wired in parallel. Each page is covered by a light valve, permitting each page to be addressed individually.

Alternatively, the light valve is omitted and the photoconductor and column-patterned electrode-over-ink layers are addressed discretely for each page, again permitting each page to be addressed individually.

15 The principles described above are especially useful when applied to flexible bistable displays and permit a flexible book-like or newspaper-like device to be created in which the various portions of the device are imaged one at a time; the loss of power to an already-addressed region does not result in a loss of image. Driver costs are minimized by enabling more than two addressing dimensions. The
20 techniques described herein are also useful for any photoconductively-addressed display. Nevertheless, it will be seen by one skilled in the art that the same principles may be applied to non-flexible displays. In addition, the same principles may be applied to non-bistable displays such as passively addressed LCD's to reduce driver costs if the refresh rate experienced by a given pixel is sufficiently
25 fast.

Several of the addressing methods referenced above require that the display be addressed sequentially in a row-by-row manner. Thus the image update rate is limited by the switching speed of the electro-optic medium. Attention will now be directed to the second main aspect of the present invention, namely
30 addressing algorithms that can speed the apparent update rate of a bistable display.

An array of island capacitors may be introduced in association with the addressing array. These capacitors can be associated with individual pixels or with cluster-level logic structures as described above. Through passive XY addressing, positive or negative charge is transmitted into the array of capacitors in a pattern matching the desired pixel image. The capacitor array may be formed by printing an electrode, a dielectric and a top electrode, either on to the ink layer or on to the photoconductor layer, or as a separate sheet that is interposed and laminated, or as part of a TFT or other logic array.

In another process, the control circuitry stores the state of the display in memory and identifies the frame-to-frame changes between each update of the display image. Only the changes are imaged, i.e., only the pixels which are changed between two adjacent frames are addressed. For small changes, such as caused by a blinking cursor or a moving mouse against a constant background, the result may be a very fast updating time.

In another process, control circuitry identifies rows that require identical column switching impulses. All such rows are activated at the same time, so that the column electrodes address all these rows simultaneously. Thus, a checkerboard graphic for any arbitrary number of rows may be imaged in at most $k*2$ seconds, where k is the switch time for the electro-optic medium.

In another process, the display is first set all white (or black), and then halfway between black and white. This may occur in $k + k/2$ seconds. As each row is thereafter addressed, the necessary addressing time for that row is at most $k*0.5$ seconds. The addressing time is therefore decreased to $k + k/2 + k*0.5$ seconds. For displays with many rows, this cuts addressing time essentially in half. Note that by halfway between black and white is meant a state where the time to switch all black and the time to switch all white are equal. If the rise and fall times of the display are different this may not be at the 50% gray level.

Thus, with a relatively simple algorithm, switching times may be greatly reduced. There are many algorithms by which pre-processing could reduce

overall addressing time for the display. It is helpful to introduce some definitions to describe these algorithms:

5 The current value of any pixel may be described on a scale of 0 to 1 where 0 = black and 1 = white. In a bistable display, these states persist until the row is re-imaged. Similarly, each pixel (x, y) may be described as having a starting state $s(x,y)$ and desired finishing state $f(x,y)$ with a difference of $d(x,y)$. Thus, the difference between the display's current and desired state may be described as a matrix array of values ranging from -1 (from white to black) to +1 (from black to white).

10 The row switch *time* vector may be defined as the maximum absolute value in each row times k seconds. The time required to address the display in a straightforward row by row fashion is the sum of the values of the row switch time vectors of the individual rows. Similarly, the row switch *direction* may be defined as a function of the highest value in the row (H) and the lowest value of the row (L).
15 Assuming the display switches from white to black with speed A and from black to white with speed B , the direction vector may be calculated as:

$$(B*H+A*L)/(A+B).$$

Assuming symmetric switching times, this simplifies to the midpoint between the high and the low. In short, if the row is all white and needs to turn all black, its
20 switch direction is -1. However if the row is black on odd columns and white on even columns, and these must each reverse, the high is 1, the low is -1, and the switch direction is 0. The switch direction represents the value for which, if all pixels in the entire row were changed by that value, the row switch time would be minimized.

25 For example, if a row starts at $[0, 0.1, 0]$ and finishes at $[1, 0.9, 1]$ the difference vector for that row is $[1, 0.8, 1]$. The row switch time is $k*1 = k$ seconds. The row direction is the midpoint between 1 and 0.8 or 0.9. If the row experienced a switch impulse increasing all pixels by 0.9, the row would be $[0.9, 1, 0.9]$ and the new difference vector would be $[0.1, -0.1, 0.1]$. The new switch time would be $0.1*k$

seconds, and the new switch direction would be 0. If only one row were addressed in this way, the total elapsed time would be $0.9*k$ plus $0.1*k$, or k seconds.

(Note that the switch direction is calculated based on the extreme high and low values ("the outliers"), since the switch time must be sufficient on each row for the very last pixel to finish switching. However, a more complex variation of this algorithm would involve calculation of the distribution of values across the row and determining whether it would be better to exclude some values in order to address the bulk of the row and then return to these excluded values at a later time.)

In one process of this invention, the vector describing the row switch direction for each row is calculated. All rows have switch directions ranging from -1 to +1. Next, the average value of all switch directions is calculated as P. All rows are activated and an impulse of P is applied. Next, all rows that started with a switch direction below P are identified. The average remaining switch direction of these rows is Q. These rows are activated and a switch impulse of Q is applied. Next, the rows that started with switch direction above P are identified. The average remaining switch direction of these rows is R. These rows are activated and a switch impulse of R is applied.

At this stage, all rows have switch directions ranging from $-1+Q$ to $1-R$. That is, the switch directions for all rows have come closer to 0 in just 3 cycles, taking less than $k*3$ seconds.

In a variation to this technique, the steps may cease after the impulse of P or the impulse of Q is applied. In another variation of the technique, each impulse P, Q and R is applied to all rows for which the net result of the impulse is to move the row's switch direction closer to zero.

These steps may be repeated for N iterations, where N is any arbitrary real number. The display is then imaged in a standard row by row fashion. In a further variant of the process, the iterations continue until Q and R are close to zero. It may readily be seen that the above techniques may be combined where appropriate to achieve faster switching times in a single display.

In the technique above, groups of rows were treated, but not groups of columns. Groups of columns may be treated using the same principles and the effects of the treatment of groups of rows and columns combined for overall faster addressing. For example, the values P, Q, and R, as defined above for rows, may be calculated. The values P', Q', and R' are also calculated in a similar manner for column switch directions. The maximum (in absolute terms) is determined among Q, Q', R, and R'. If Q or R is the maximum, that switch impulse is applied to all columns across designated rows. If Q' or R' is the maximum, that switch impulse is applied to all rows across designated columns. This process may be repeated for N iterations.

In a variation of this process, if Q or R is the maximum for example, the switch impulse of Q is applied to all columns against the associated rows, and then the switch impulse of R is applied to all columns against its associated rows. All 4 values Q, Q', R, R' are then recalculated, and the process may be repeated for N iterations.

Either method desirably proceeds until Q, Q', R, and R' are all close to zero. It will readily be apparent that if addressing using three or more dimensions is employed in any of the ways described above, the technique described in the foregoing passage may be extended to one or more additional dimensions by calculating values Q'' and R'' as well.

The selection of a specific method for a given display design may be affected by numerous factors, including the ratio of rows and columns, the relative number of rows as compared to switching speed, and by the processor power available for pre-processing, among other factors.

In another general approach, orthogonal wave functions such as are used for active addressing of LCD's are employed, adjusting (if necessary) for the bistable/multi-stable memory effect of electrophoretic and similar displays by calculating the difference in position required. These functions have a further advantage in that they have been implemented in silicon and may be simpler to

calculate than a more complex approach. A variation may further be employed that takes into account the additional dimension of Z addressing.

5 It will readily be apparent to those skilled in the display art that the techniques described could also be used more generally to address any kind of passive display with memory effect.

10 From the foregoing description, it will be seen that the displays and processes of the present invention permit the number of drivers needed in a display to be greatly reduced, and provide processes by which electronic, light-emitting and light valve apparatus can usefully be combined to address a display. The present invention also provides several processes which substantially reduce the switching time of bi- and multi-stable displays.

15 While the invention has been particularly shown and described with reference to specific preferred embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS

1 1. An electronic display (10; 20; 100; 50; 200; 230; 240; 250)
2 comprising an electro-optic material having a plurality of pixels (14, 16), and
3 separate first (X1; 122, 124, 126; r1, r2, r3; r1, r2, r3, r4), and second (Y1, Y2; 210)
4 sets of addressing means for addressing the pixels (14, 16), each of the pixels (14,
5 16) being associated with one addressing means in each of the two sets, such that
6 any specific pixel (14, 16) can be addressed by application of signals within
7 predetermined ranges to each of the two addressing means associated with that
8 specific pixel (14, 16), the display (10; 20; 100; 50; 200) being characterized by a
9 third set of addressing means (12; 128, 130; z1, z2; c1, c2, c3, c4) separate from the
10 first and second sets (X1, Y1, Y2; 122, 124, 126; r1, r2, r3; r1, r2, r3, r4, 210), each
11 of the pixels (14, 16) also being associated with one addressing means of the third
12 set (12; 128, 130; z1, z2; c1, c2, c3, c4), such that any specific pixel (14, 16) can be
13 addressed by application of signals within predetermined ranges to each of the three
14 addressing means associated with that specific pixel (14, 16).

1 2. An electronic device according to claim 1 wherein said pixels
2 are arranged in a plurality of sub-arrays, each pixel within any specific sub-array
3 being associated with one of the first (122, 124, 126; r1, r2, r3) and second sets of
4 addressing means, the third set of addressing means (128, 130; z1, z2) having the
5 form of a plurality of switching means, at least one of the switching means being
6 associated with each of the sub-arrays, the switching means (128, 130; z1, z2)
7 associated with each sub-array having an off state, in which signals on at least one of
8 the first (122, 124, 126; r1, r2, r3) and second sets of addressing means are
9 prevented from reaching the associated sub-array, and an on state, in which signals
10 from both the first (122, 124, 126; r1, r2, r3) and second sets of addressing means
11 are permitted to reach and address the associated sub-array.

1 3. An electronic display according to claim 2 characterized by
2 control means arranged to control the switching means (128, 130; z1, z2) so that
3 only the switching means (128, 130; z1, z2) associated with one sub-array is in its
4 on state at any given moment.

1 4. An electronic display according to claim 2 or 3 characterized
2 in that each sub-array comprises a discrete page (P1, P2), the pages (P1, P2) formed
3 by the plurality of sub-arrays being stacked on top of each other so that the entire
4 display (50) forms a multi-page electronic book.

1 5. An electronic display according to claim 4 characterized by
2 conductive vias (52) extending between adjacent pages (P1, P2) and connecting at
3 least one of the first (r1, r2, r3) and second sets of addressing means on the adjacent
4 pages (P1, P2).

1 6. An electronic display according to any one of the preceding
2 claims characterized in that the first second and third sets of addressing devices all
3 have the form of electrical conductors and/or electronic devices.

1 7. An electronic display according to any one of the preceding
2 claims characterized in that at least one of the sets of addressing devices comprises a
3 photoconductor (206).

1 8. An electronic display according to claim 7 characterized by a
2 light source (202) associated with the photoconductor (206) and selectively operable
3 to switch the photoconductor (206) between a conductive and a non-conductive
4 state.

1 9. An electronic display according to claim 7 characterized by a
2 light source (202) associated with the photoconductor (206) and a light valve (204)
3 disposed between the light source (202) and the photoconductor (206) and arranged
4 to control transmission of light from the light source (202) to the photoconductor
5 (206).

1 10. An electronic display according to claim 9 characterized in
2 that the light valve (204) comprises a polymer-dispersed liquid crystal.

1 11. An electronic display according to any one of claims 8, 9 and
2 10 characterized in that the light source (202) comprises an electroluminescent
3 material.

1 12. An electronic display (240) according to claim 9 characterized
2 by a plurality of light sources arranged as a series of elongate rows (r1, r2), and a

3 plurality of light valves arranged as series of elongate columns crossing the elongate
4 rows, the light sources and light valves together defining a two-dimensional array of
5 pixels in the photoconductor.

1 13. An electronic display according to claim 9 characterized by a
2 plurality of pages stacked on top of one another to form a multi-page electronic
3 display, each page having a single light source and a single light valve, so that the
4 page or pages to be written at any given moment are selected by controlling the state
5 of the light valves.

1 14. An electronic display (230; 240; 250; 260) according to claim
2 9 characterized in that the first addressing means (c1, c2; c1, c2, c3, c4) comprises a
3 plurality of electrical conductors and means for applying potentials selectively to
4 these conductors, the second addressing means (r1, r2) comprises a plurality of light
5 emitting devices and means for generating light selectively from these light emitting
6 devices, and the third addressing means comprises a plurality of light valves (z1, z2;
7 z1, z2, z3) and means for selectively setting the light valves (z1, z2; z1, z2, z3) to
8 their transmissive or non-transmissive states.

1 15. An electronic display (240) according to any one of the
2 preceding claims characterized by three sets of pixels arranged to display different
3 colors, the third set of addressing means (z1, z2, z3) being arranged to select one of
4 the three sets of pixels to be addressed at any given moment.

1 16. An electronic display according to any one of the preceding
2 claims characterized by a fourth set of addressing means for addressing the pixels,
3 the fourth set being separate from the first, second and third sets of addressing
4 means, each of the pixels of the display being associated with one addressing means
5 in each of the four sets, such that any specific pixel of the display can be addressed
6 by application of signals within predetermined ranges to each of the four addressing
7 means associated with that specific pixel.

1 17. An electronic display according to any one of the preceding
2 claims characterized in that the electro-optic material comprises an electrophoretic
3 medium.

1 18. An electronic display according to claim 17 characterized in
2 that the electrophoretic medium is an encapsulated electrophoretic medium.

1 19. An electronic display comprising an electro-optic material
2 having a plurality of separately addressable pixels wherein the number of driver
3 outputs to the pixel array is less than the square root of the number of pixels.

1 20. A method of addressing an electronic display, the method
2 being characterized by:

3 providing an electro-optic material having a plurality of pixels;

4 providing first, second and third sets of addressing means for
5 addressing the pixels, each of the pixels being associated with one addressing means
6 in each of the three sets; and

7 applying predetermined signals to the three addressing means
8 associated with a specific pixel, thereby addressing that pixel.

1 21. A method of addressing a bistable electronic display having a
2 plurality of pixels arranged in an array comprising a plurality of rows and plurality
3 of columns, the method comprising selecting a plurality of rows or columns and
4 applying a simultaneous and equivalent switching impulse to all selected rows and
5 columns.

1 22. A method of addressing a bistable electronic display having a
2 plurality of pixels arranged in a plurality of rows, the method being characterized
3 by:

4 (a) comparing a starting state of the display with a desired finishing
5 state and determining for each pixel a change value representative of the change
6 needed to change the starting state of that pixel to its desired finishing state; and

7 (b) calculating from the pixel change values for each row, a switch
8 direction value for that row, this switch direction value representing the value for
9 which, if all pixels of that row were changed by the switch direction value, the row
10 switch time required to switch the row to the desired finishing state would be
11 minimized.

1 23. A method according to claim 22 further comprising any one
2 or more of the following steps:

3 (c) calculating the average switch direction value for all rows of the
4 display;

5 (d) identifying all rows with switch direction values less than the
6 average switch direction value calculated in step (c);

7 (e) calculating the average switch direction value of all rows
8 identified in step (d);

9 (f) applying to all rows identified in step (d) an impulse sufficient to
10 cause a change in state equal to the average switch direction value calculated in step
11 (e);

12 (g) identifying all rows with switch direction values greater than the
13 average switch direction value calculated in step (c);

14 (h) calculating the average switch direction value of all rows
15 identified in step (g); and

16 (i) applying, to all rows identified in step (g), an impulse sufficient to
17 cause a change in state equal to the average switch direction value calculated in step
18 (g).

1 24. A method of addressing a bistable electronic display having a
2 plurality of pixels each having a first display state, a second display state differing in
3 at least one optical characteristic from the first display state, and a plurality of
4 intermediate states having values of the optical characteristic intermediate those of
5 the first and second display states, the method being characterized by:

6 driving all the pixels of the display to the same one of the
7 intermediate states; and

8 thereafter addressing the pixels individually to drive them to their
9 desired states.

1 25. A method of addressing a bistable electronic display having a
2 plurality of pixels arranged in a plurality of rows and columns, the method being
3 characterized by:

- 4 (a) comparing a starting state of the display with a desired finishing
5 state and determining for each pixel a change value representative of the change
6 needed to change the starting state of that pixel to its desired finishing state;
7 (b) comparing the change values of pixels in differing rows but the
8 same column and locating at least two pixels having the same change value; and
9 (c) addressing these least two pixels having the same value
10 simultaneously by addressing the rows and the column on which these pixels are
11 located.

1 26. A method of addressing a bistable electronic display having a
2 plurality of pixels, the method being characterized by:

- 3 comparing a starting state of the display with a desired finishing state
4 and determining which pixels differ between the two states; and
5 addressing only those pixels which differ between the two states.

1 27. A method of addressing a bistable electronic display having a
2 plurality of pixels, the method being characterized by:

- 3 providing an array of island capacitors associated with the pixels of
4 the display;
5 through passive matrix XY addressing, introducing electrical charge
6 into the capacitors in a pattern matching the image desired on the display; and
7 thereafter allowing the charges on the capacitors to complete the
8 addressing of the pixels of the display.

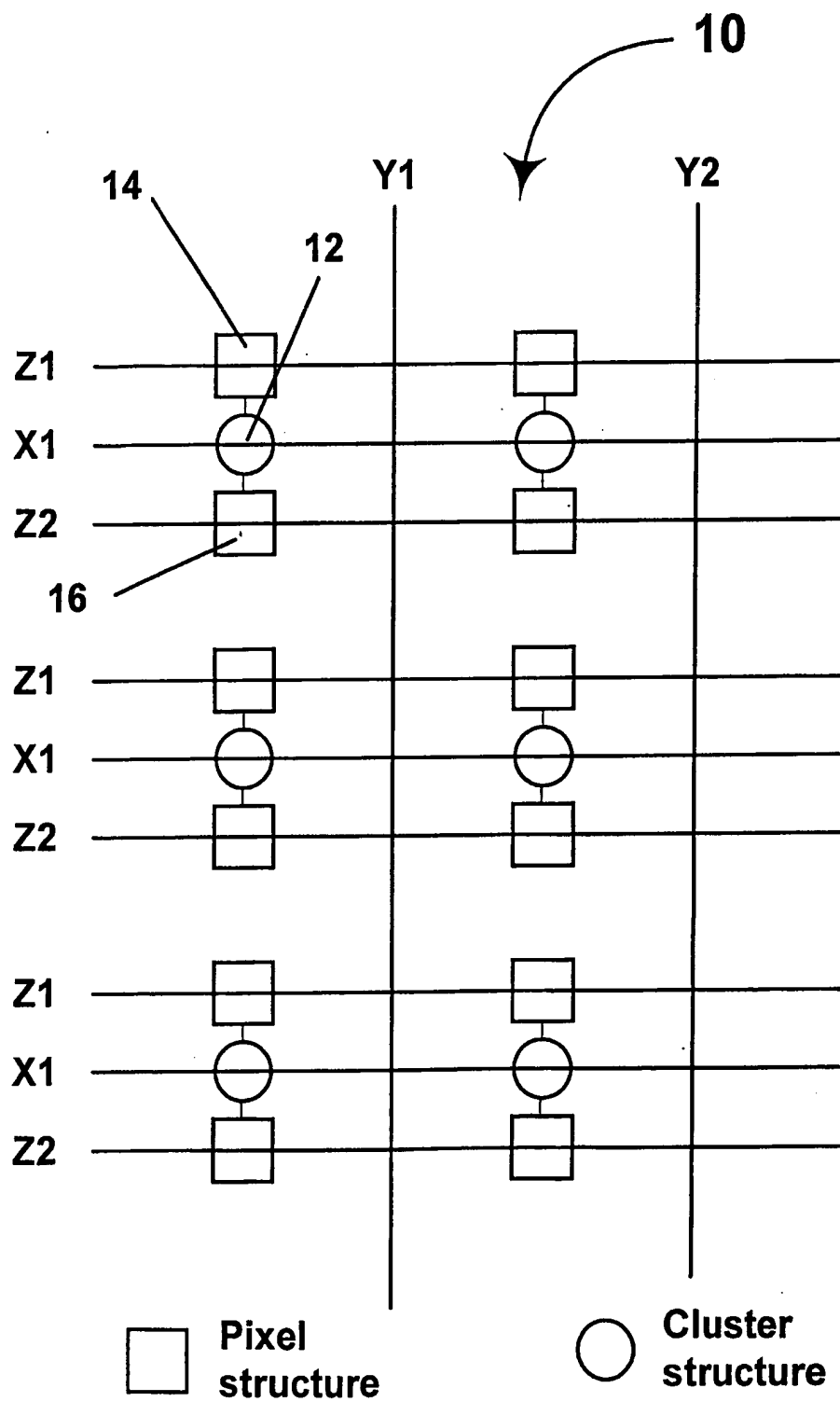


Fig. 1

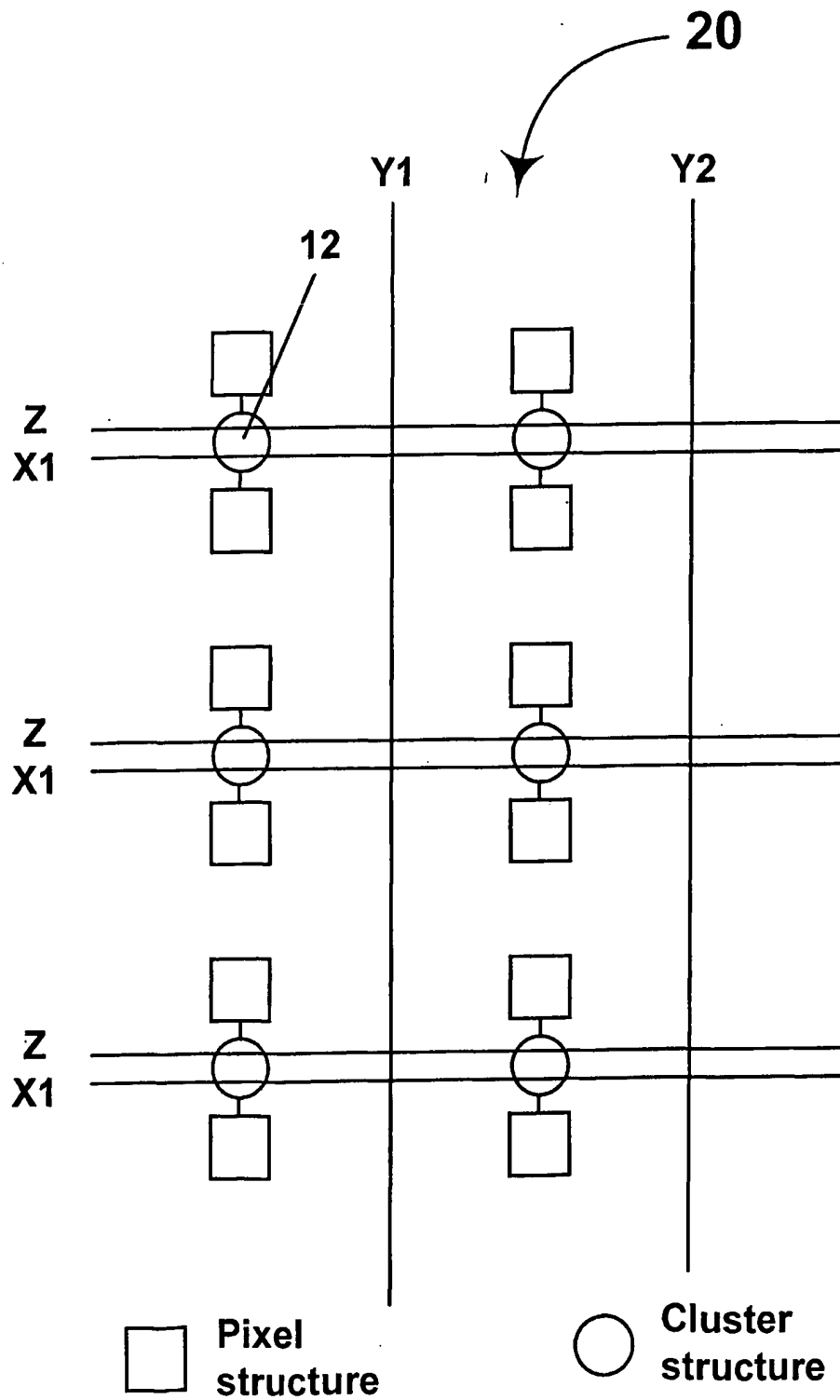
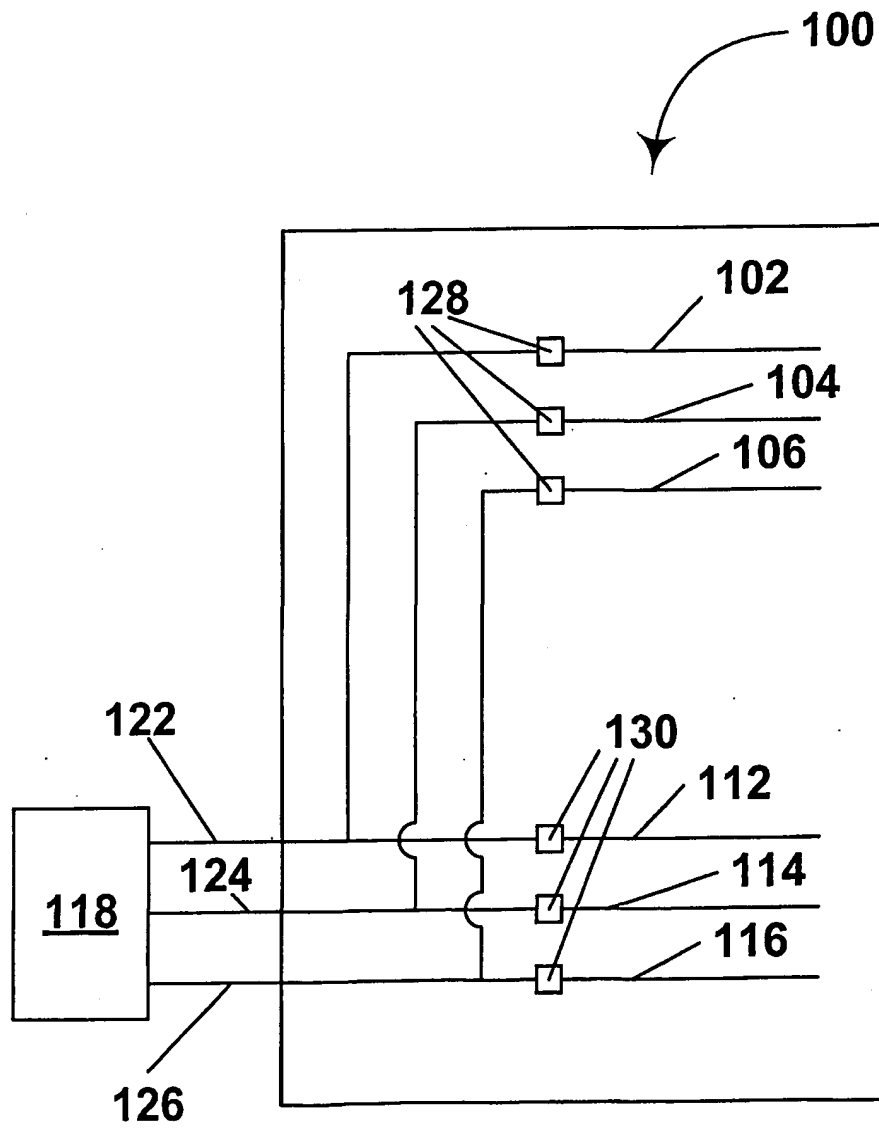
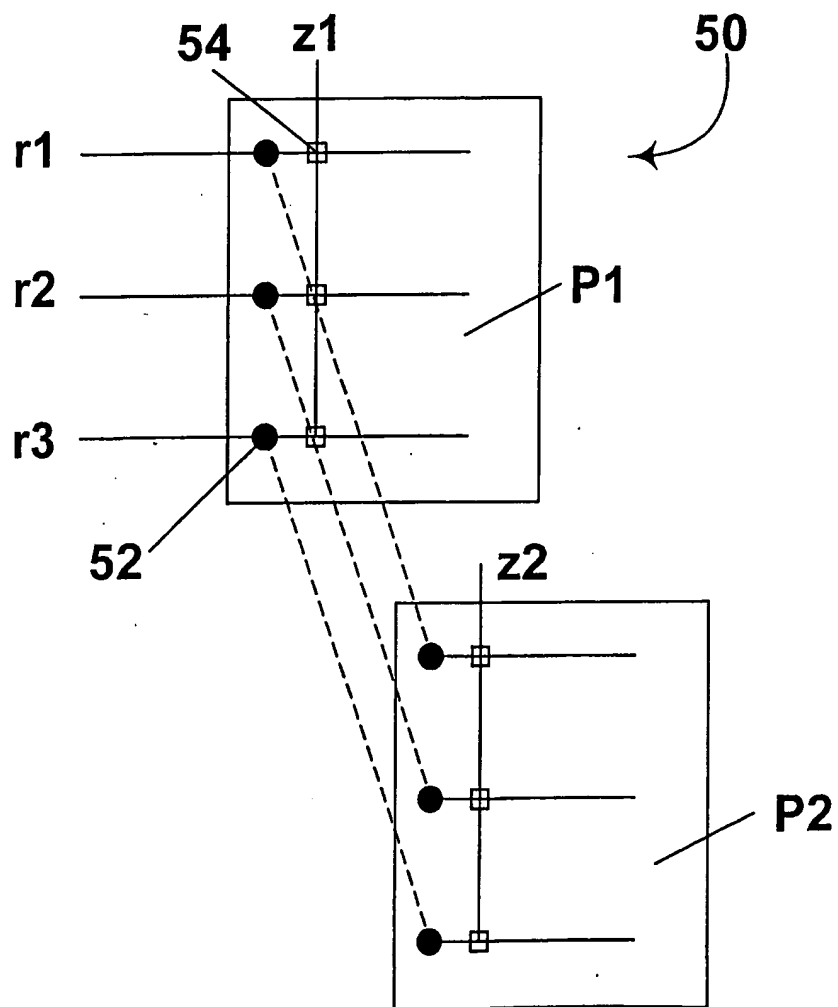


Fig. 2

**Fig. 3**

**Fig. 4**

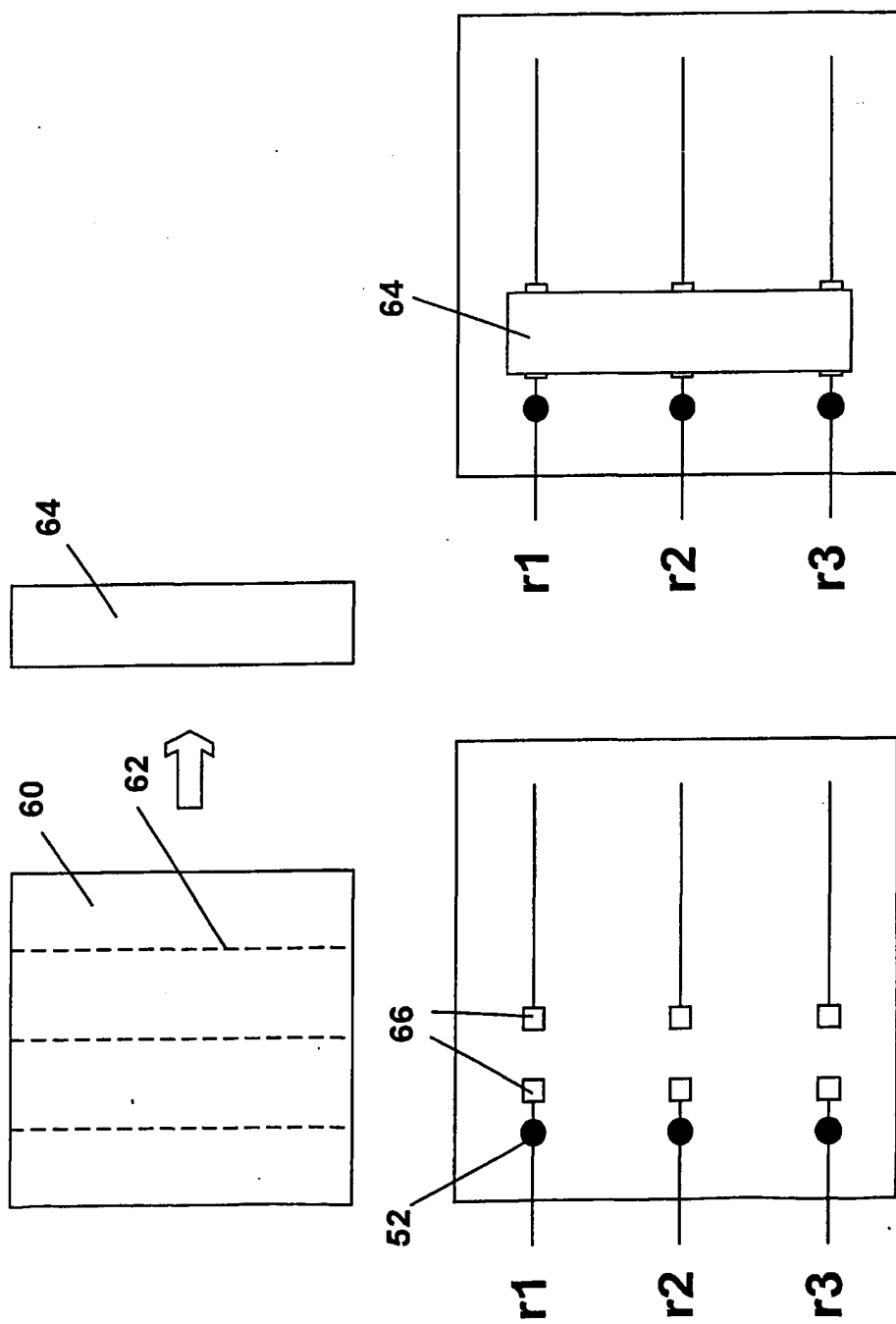


Fig. 5A

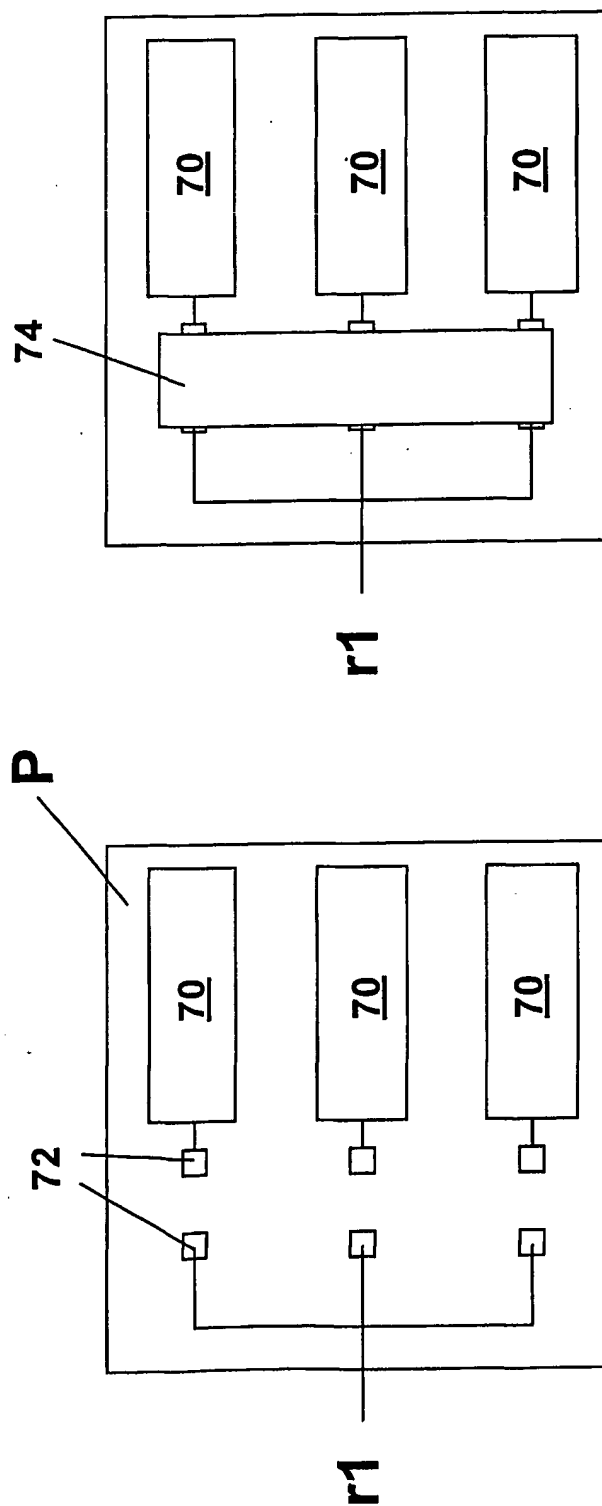


Fig. 5B

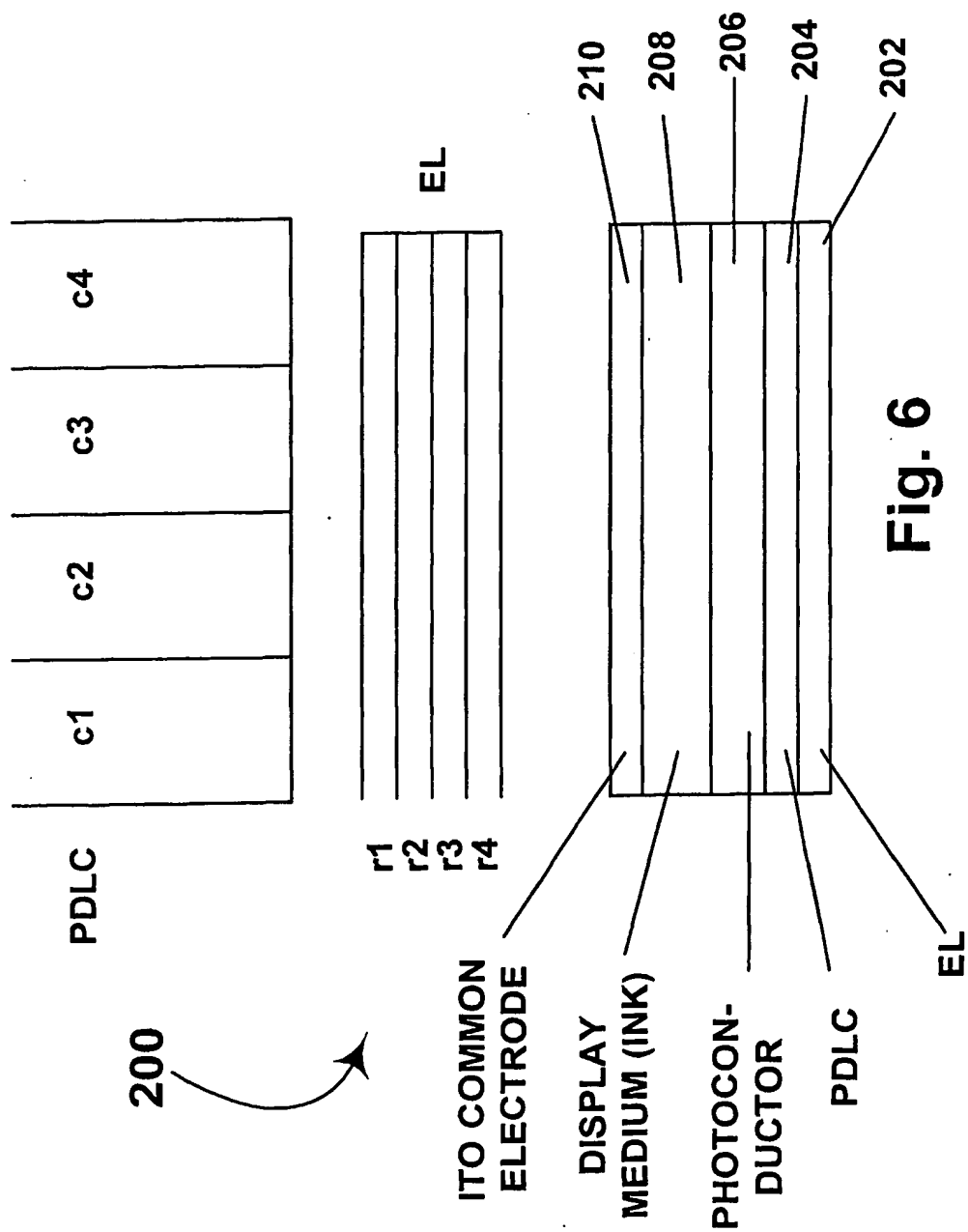


Fig. 6

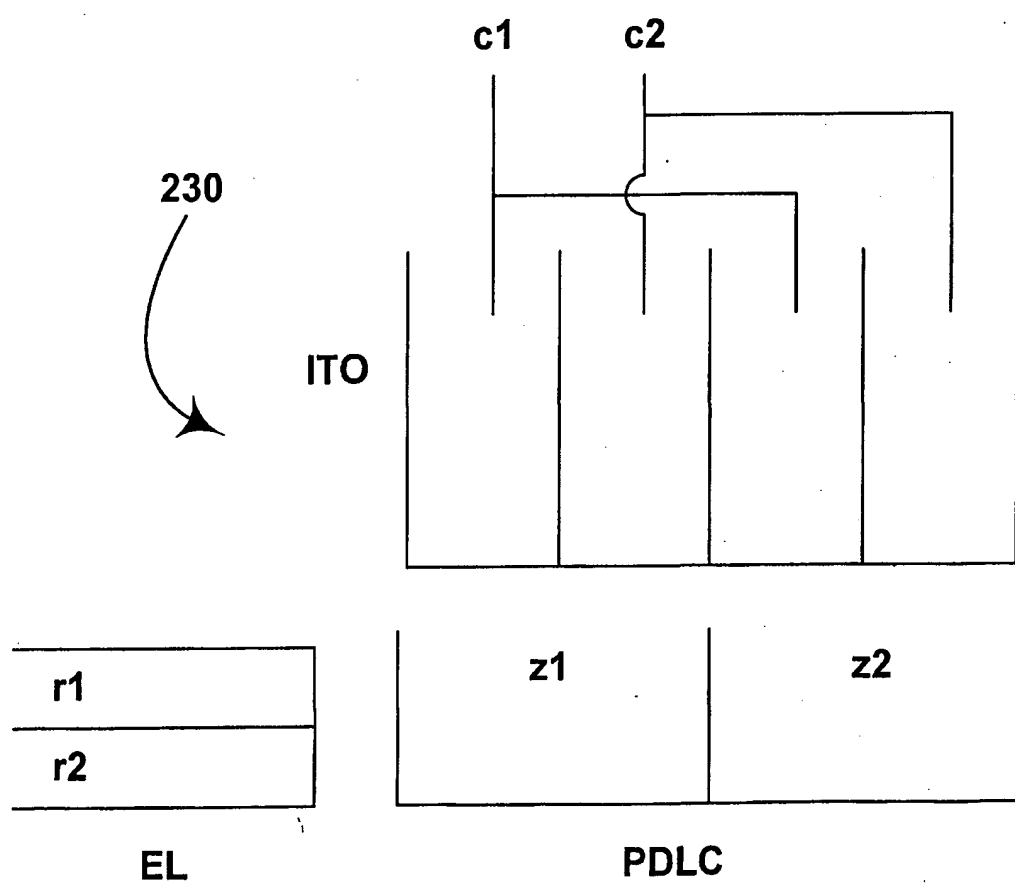


Fig. 7

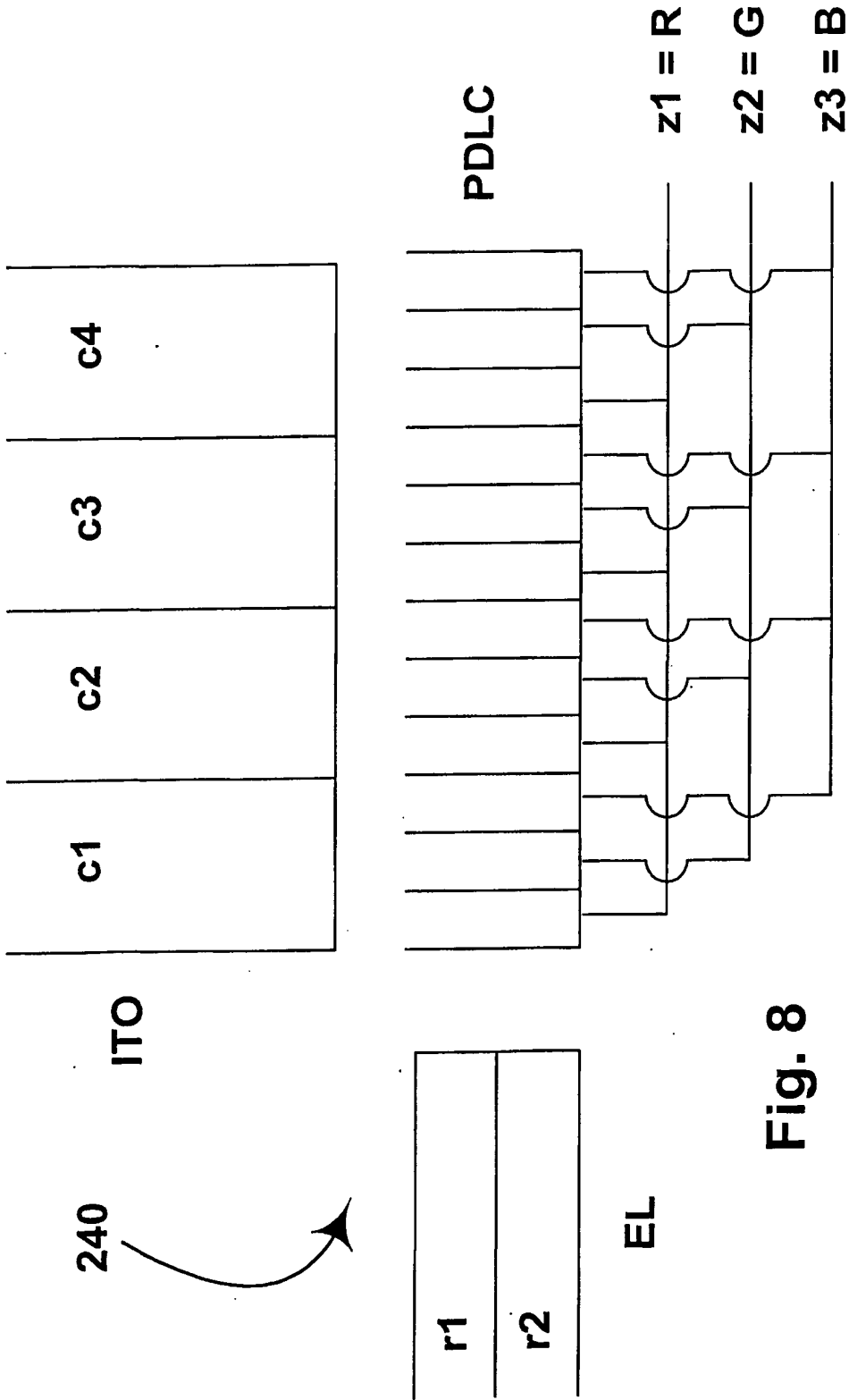


Fig. 8

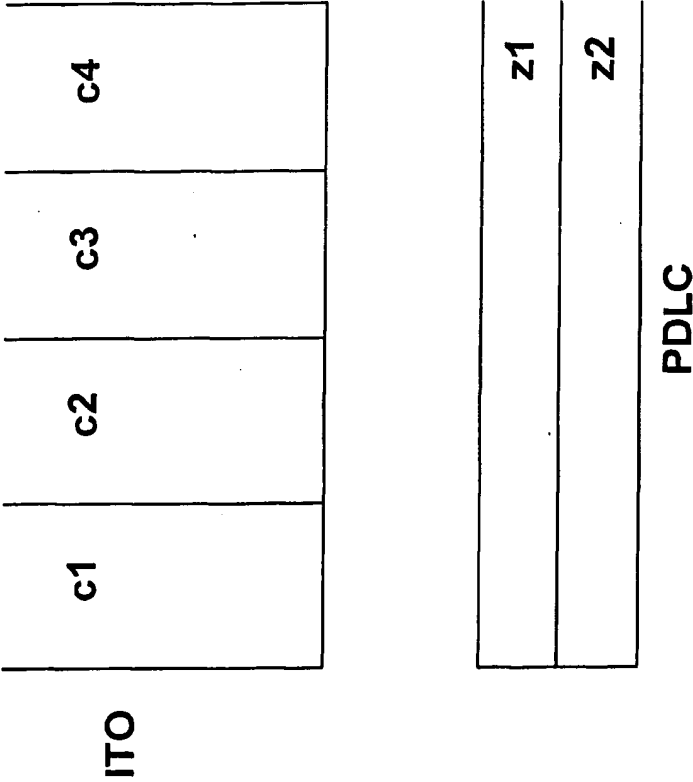
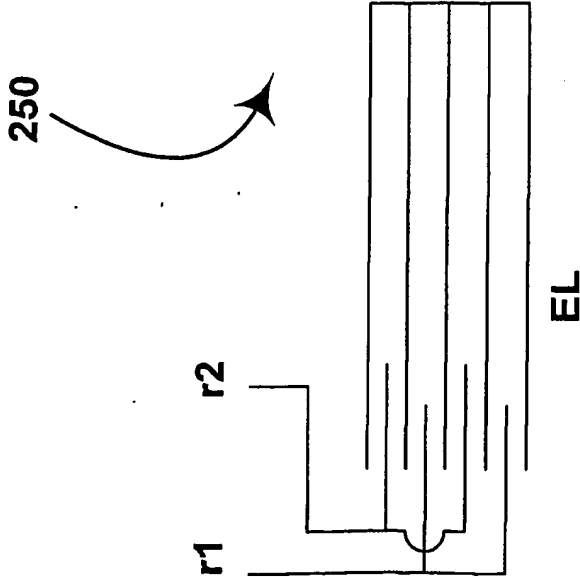


Fig. 9



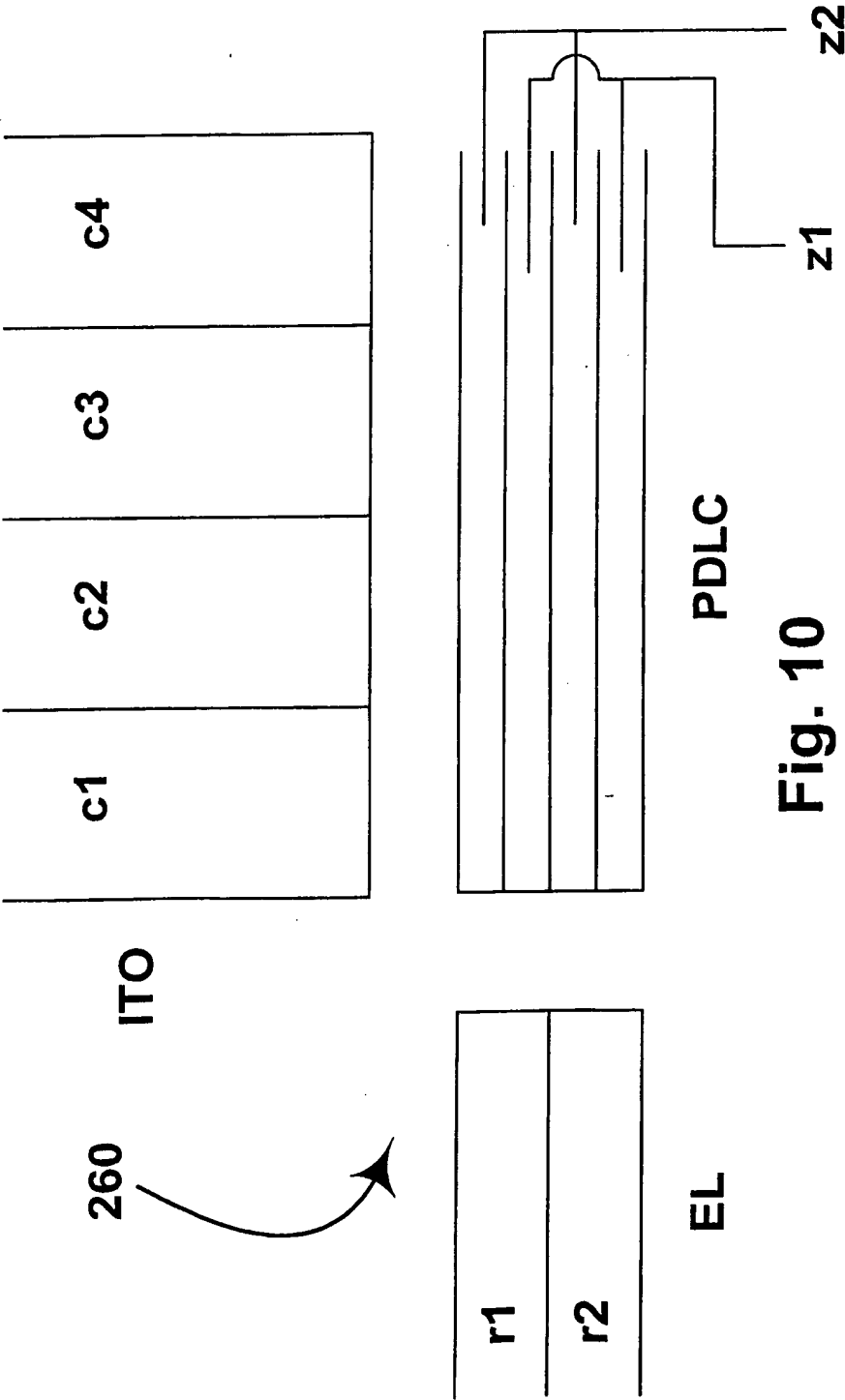


Fig. 10